Reference Design RD-402

1. Fairchild Motion SPM® 5 SuperFET® Series

This reference design supports designs using Fairchild’s Motion SPM® 5 SuperFET® series of products. It should be used in conjunction with the SPM 5 SuperFET series datasheets and Fairchild’s technical support team. Please visit Fairchild’s website at http://www.fairchildsemi.com.

<table>
<thead>
<tr>
<th>Application</th>
<th>Fairchild Devices</th>
<th>Input Voltage Range</th>
<th>Typical Power Rating</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Home Appliance (Refrigerator)</td>
<td>FSB50660SF, FSB50660SFT, FSB50760SF, FSB50760SFT</td>
<td>300~400 V&lt;sub&gt;DC&lt;/sub&gt;</td>
<td>150 W~200 W</td>
<td>3-Phase Inverter</td>
</tr>
</tbody>
</table>

**Key Features**

- 600 V $R_{DS(ON)}$=530 mΩ / 700 mΩ (Max.) 3-Phase SuperFET Inverter Bridge, including High Voltage Integrated Circuit (HVIC)
- 3 Divided Negative DC-Link Terminals for Inverter Current-Sensing Application
- HVIC for Gate Driving and Under-Voltage Lockout (UVLO) Protection
- Optimized for Low Electromagnetic Interference
- Embedded Bootstrap Diode in Package
- Integrated Temperature-Sensing Function (Linear Voltage Output by Temperature) in HVIC
- Isolation Voltage Rating of 1500 V<sub>RMS</sub> for 1 Minute
2. Schematics

Figure 1. Block Diagram of Compressor Driver for Refrigerator
Figure 2. Schematic of Reference Design for 3-Phase Inverter Key Parameter Design
3. **Key Parameter Design**

3.1. **Selection of Bootstrap Capacitance (CBS)**

The bootstrap capacitor can be calculated by:

\[
C_{BS} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}}
\]  

(1)

where:

- \( \Delta t \) = maximum on pulse width of high-side MOSFET;
- \( \Delta V_{BS} \) = the allowable discharge voltage of the CBS (voltage ripple); and
- \( I_{Leak} \) = maximum discharge current of the CBS.

Normally, \( I_{Leak} \) consist of the following items:

- Gate charge for turning the high-side MOSFET turn on
- Quiescent current to the high-side circuit in the HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- \( C_{BS} \) capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 1 mA of \( I_{Leak} \) is recommended (operating \( V_{BS} \) supply current).

Calculation example of \( C_{BS} \):

\[
C_{BS\_min} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} = \frac{1mA \times 2.6ms}{0.2V} = 10 \times 10^{-6}
\]  

(2)

where:

- \( I_{Leak} = 1 \) mA (recommended value);
- \( \Delta V_{BS} = 0.2 \) V (depends on system);
- \( \Delta t = 2.6 \) ms (depends on system);
- More than 2~3 times \( \rightarrow \) 20~30 \( \mu \)F \( \rightarrow \) standard nominal capacitance 22 \( \mu \)F.
3.2. Initial Charging Sequence for Bootstrap Capacitor

Figure 3 is built-in bootstrap diode I_d-V_f characteristic in FSB50760SF.

The built-in bootstrap diodes of the Motion SPM® 5 SuperFET® series have equivalent resistance characteristic by special I_d-V_f characteristics. Therefore, circuit engineers only need external bootstrap capacitor for bootstrap circuit.

The bootstrap capacitors should be fully charged for the supply voltage of HVIC by the turn-on low-side MOSFET and the gate voltage of the high-side MOSFET; otherwise, the high-side MOSFET is operated in high-dissipation mode. For one bootstrap capacitor (C_BS), when charged initial charging current (I_BS) flows through low-side MOSFET and I BS is approximately 1.0 A. Figure 4 is bootstrap capacitor charging waveform and Figure 5 is bootstrap capacitor charging time by bootstrap capacitor value (t_charge at V_BS=12.0 V).

To charge three bootstrap capacitors at the same time; theoretically, the maximum initial charging current is around 3.0 A. In this case, this I_BS could be lead to a SCP (OCP) error. Therefore, charge bootstrap capacitors individually, as shown in Figure 6.
Figure 5. Waveform of Bootstrap Capacitor Charge ($V_{CC}=15\,V$, $C_{BS}=47\,\mu F$, $f_{SW}=5.0\,kHz$, $T_J=25^\circ C$)

Figure 6. Recommended Initial Bootstrap Capacitors Charging Sequence

$V_{IN(UL)}$: 5.0V/div $I_{BS}$: 0.2A/div $V_{BS}$: 5.0V/div

Time: 500\,\mu s/div
3.3. Selection of Shunt Resistor

The value of shunt resistor is calculated by the following equations.

Maximum Short Circuit (SC) current trip level (depend on user selection):

\[ I_{SC\text{(max)}} = 1.5 \times I_d \text{ (rated current)} \]  \hspace{1cm} (3)

SC trip reference voltage (depend on user selection):

\[ V_{SC} = \min\{0.45 \text{ V, typ.0.5 \text{ V, max.0.55 \text{ V}}\} \text{ (Tolerance 10%, depends on system)} \]  \hspace{1cm} (4)

Shunt resistance:

\[ I_{SC\text{(max)}} = V_{SC\text{(max)}} / R_{SHUNT\text{(min)}} \rightarrow R_{SHUNT\text{(min)}} = V_{SC\text{(max)}} / I_{SC\text{(max)}} \]  \hspace{1cm} (5)

If the deviation of shunt resistor is limited below ±5%:

\[ R_{SHUNT\text{(typ)}} = R_{SHUNT\text{(min)}} / 0.95, \ R_{SHUNT\text{(max)}} = R_{SHUNT\text{(typ)}} \times 1.05 \]  \hspace{1cm} (6)

Actual SC trip current level becomes:

\[ I_{SC\text{(typ)}} = V_{SC\text{(typ)}} / R_{SHUNT\text{(typ)}}, \ I_{SC\text{(min)}} = V_{SC\text{(min)}} / R_{SHUNT\text{(max)}} \]  \hspace{1cm} (7)

The power rating of shunt resistor is calculated by the following equation:

\[ P_{SHUNT} = (I_{rms}^2 \times R_{SHUNT} \times \text{Margin}) / \text{Derating Ratio} \]  \hspace{1cm} (8)

where:

- \( I_{rms} \) = Maximum load current of inverter;
- \( R_{SHUNT} \) = Shunt resistor typical value at \( T_C=25\^\circ\text{C} \);
- Derating Ratio of shunt resistor at \( T_{SHUNT}=100\^\circ\text{C} \) (from datasheet of shunt resistor); and
- Safety margin (determined by customer).

Value of Shunt Resistor Calculation Examples

Calculation Conditions:

- **DUT**: FSB50760SF, Tolerance of \( R_{SHUNT} \): ±5%
- SC trip reference voltage:
  \[ V_{SC\text{(min)}}=0.45 \text{ V, } V_{SC\text{(typ)}}=0.50 \text{ V, } V_{SC\text{(max)}}=0.55 \text{ V} \]
  where:
  \[ I_{SC\text{(max)}}: 1.5 \times 1.5 = 2.25 \text{ A} \]
  \[ R_{SHUNT\text{(min)}}: V_{SC\text{(max)}} / I_{SC\text{(max)}} = 0.55 \text{ V} / 2.25 \text{ A} = 0.24 \Omega \]
  \[ R_{SHUNT\text{(typ)}}: R_{SHUNT\text{(min)}} / 0.95 = 0.24 \Omega / 0.95 = 0.26 \Omega \]
  \[ R_{SHUNT\text{(max)}}: R_{SHUNT\text{(typ)}} \times 1.05 = 0.26 \Omega \times 1.05 = 0.27 \Omega \]
  \[ I_{SC\text{(min)}}: V_{SC\text{(min)}} / R_{SHUNT\text{(max)}} = 0.45 \text{ V} / 0.27 \Omega = 1.67 \text{ A} \]
  \[ I_{SC\text{(typ)}}: V_{SC\text{(typ)}} / R_{SHUNT\text{(typ)}} = 0.50 \text{ V} / 0.26 \Omega = 1.94 \text{ A} \]

Power Rating of Shunt Resistor Calculation Example

Calculation Conditions:

- Maximum load current of inverter (\( I_{rms} \)): 1.0 \text{ A}_{rms} 
- Shunt resistor value at \( T_C=25\^\circ\text{C} \) (\( R_{SHUNT} \)): 0.27 \Omega
- Derating ratio of shunt resistor at \( T_{SHUNT}=100\^\circ\text{C} \): 70%
- Safety margin: 20%
- \( P_{SHUNT} = (I_{rms}^2 \times R_{SHUNT} \times \text{Margin}) / \text{Derating Ratio} = (0.82 \times 0.27 \times 1.2) / 0.7 = 0.46 \text{ W} \)

(Therefore, recommended power rating of shunt resistor is 1.0 W).
3.4. Design of Short-Circuit Current Protection (SCP) Circuit

Figure 7 and Figure 8 are typical application circuits for SCP function. Figure 7 (using MCU), needs external comparator circuits. Figure 8 (using BLDC controller, such as FCM8531 with an OCP function), needs no external circuits.

![Short-Circuit Current Protection (SCP) Circuit Using MCU](image1)

Figure 7. Short-Circuit Current Protection (SCP) Circuit Using MCU

![Short-Circuit Current Protection (SCP) Circuit Using BLDC Controller](image2)

Figure 8. Short-Circuit Current Protection (SCP) Circuit Using BLDC Controller

3.5. Design of Over-Temperature Protection (OTP) Circuit

Figure 9 is V-T curve of built-in Temperature Sensing (TS) function in the HVIC of FSB50760SF. For detail information of V-T table, refer to related application note.

![V-T Curve of Temperature-Sensing (TS) Function in HVIC of FSB50760SF](image3)

Figure 9. V-T Curve of Temperature-Sensing (TS) Function in HVIC of FSB50760SF
Figure 10 is typical application circuit for temperature-sensing function. In this reference design, the set level is 100°C ($V_{TS}=2.23$ V), reset level is 80°C ($V_{TS}=1.85$ V), and hysteresis temperature is 20°C (see Figure 11). If using an Analog-to-Digital Conversion (ADC) port, only a capacitor between the VTS pin and GND is required (see Figure 12).
4. Print Circuit Board (PCB) Layout Guidance

- The capacitor between $V_{CC}$ and zener diode should be placed to SPM as close as possible.
- It is recommended to connect control GND and power GND at only a point. (Not copper pattern and don’t make a loop in GND pattern). And wiring should be as short as possible.
- The main electrolytic capacitor should be placed to snubber capacitor as close as possible.
- Wiring between $N_{P}, N_{V}$, and $N_{W}$ should be as short as possible.
- Place snubber capacitor between $P$ and terminal as close as possible.

**Figure 13. PCB Layout Guidance**
5. Related Resources

FSB50660SF – Motion SPM® 5 SuperFET® Series
FSB50660SFT – Motion SPM® 5 SuperFET® Series
FSB50660SFS – Motion SPM® 5 SuperFET® Series
FSB50760SF – Motion SPM® 5 SuperFET® Series
FSB50760SFT – Motion SPM® 5 SuperFET® Series
FSB50760SFS – Motion SPM® 5 SuperFET® Series
AN-9082 – Motion SPM® 5 Series Thermal Performance Information by Contact Pressure
FCM8531 – MCU Embedded and Configurable 3-Phase PMSM / BLDC Motor Controller
Fairchild Reference Designs at http://www.fairchildsemi.com/referencedesign/

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