Board-Level Evaluation of Power Quad Flat No-Lead (PQFN) Packages

Marlon D. Bartolo and Erwin Ian V. Almagro

Abstract — Evaluations in surface-mount board assembly are conducted for two new packages, the PQFN 3mm x 3mm and the PQFN 5mm x 6mm. These packages offer very low inductance for better circuit performance. The aim of this paper is to provide practical guidance regarding PCB mounting and thermal management. The processes evaluated are stencil printing, component placement, and reflow. Stencil design is shown to be the most critical. In the reflow process, exposure to temperature above its rating results in reliability risk; thus, thermocouple location is considered in temperature profiling. Temperature cycle test, drop test, vibration, and bending tests are conducted to determine the reliability of the assembly. Thermal simulation is conducted using ANSYS® software, showing the effect of voids present in the solder between the package terminals and the land pad. Recommendations for successful assembly are presented.

1. INTRODUCTION

PQFN 5x6 and PQFN 3x3 are MLP type packages with exposed die paddle. The exposed die paddle provides an advantage over conventional SOIC packages by allowing better solder joint reliability and faster heat transfer from the silicon junction to the board. This type of MLP is manufactured in a matrix-array design that results in higher throughput in package assembly. With the exposed die paddle of this MLP-type package, this paper explains how to maximize the performance in the assembly line and in applications in the field.

A typical board assembly process consists of solder paste printing on the board, component placement and reflow. Each of these processes is crucial in achieving good board assembly. For the PQFN packages, the design of the stencil aperture for solder paste printing is critical. Several types of assembly defects are associated with the design. The IPC standard recommends, at most, 25 micrometers reduction in the aperture size for the lead pads, a 20 to 50% reduction for the exposed die pad of the PQFN package. Window paning of the aperture for the exposed die pad is recommended to allow solvents and other volatile components of the solder flux to outgas easily during reflow, minimizing void formation. A study on different aperture designs with different aperture reduction for the exposed die paddle is conducted. Different stencil thicknesses are also used in the study to simulate the feasibility of using different stencil thicknesses for this type of package. Solder paste from different manufacturers are studied and evaluated to determine which aperture designs the paste suits.

With the flat-bottom structure of the PQFN packages, placement of the component on the board with printed solder pastes can be critical. Applying too much pressure on the component during placement can result in paste being squashed and spread outside the board pad, leading to bridging and beading. A simple evaluation is presented to demonstrate this. An additional evaluation was done to test if the PQFN package has the capability to align itself on the board pad. This test gives board assemblers information on the sensitivity of the package to placement offset and sets a requirement for the placement accuracy of the mounter.

Board-level performance based on industry standards are presented and discussed. The test conducted includes temperature cycle test, drop test, and board bending tests. These tests are performed to simulate field conditions for handheld and portable devices. Thermal performance and how the board design impacts its performance are also discussed. This includes experimentation on how the solder voids in board assembly affect the thermal performance. Finite element analysis, using computer aided design software, ANSYS®, is used to further analyze the effect. Worst-case conditions difficult to simulate in actual experimentation are conducted. The effect of thermal vias in pad are also presented.
II. PQFN 5x6 AND PQFN 3x3 PACKAGE ASSEMBLY AND STRUCTURE

The Power Quad Flat No-Lead (PQFN) package, also known as an MLP-type package, has been designed to meet high-power dissipation requirements of automotive, industrial, and commercial applications. It is a surface-mount, molded package with lead pads on its bottom face.

![Fig. 1. 3D Drawing of the PQFN 3x3 and the PQFN 5x6.](image)

The process assembly for Fairchild Semiconductor’s PQFN 5x6 and PQFN 3x3 includes die-attach on the copper frame substrate using a hot-soldering process. PQFN 5x6 uses a solder die attach material while the PQFN 3x3 utilizes Ag-filled epoxy. Die attach is followed by round wire-bonding or ribbon-wire bonding on the die top going to the leadpost. The wire bonding process creates an electrical connection between the gate and source of the silicon chip to the leads of the package. Since the wire material is composed of a heavy gage aluminum material, it assures good thermal and electrical connection. After wirebonding, the entire metal frame is sent to molding, where the array of units is molded into a single block. Baking is done after molding to fully cure the encapsulant material. The mold block is then singulated through sawing, then sent to electrical testing to screen out bad units.

The package standard reference of both packages are based on JEDEC MO-240, issue A, var. AA, dated October 2002.

A. Solder Paste Printing and Stencil Design

Several defects in board assembly are attributed to the printing process and its stencil design. In the case of PQFN board assembly; solder beading, bridging, open lead connection due to tilting, and inconsistent paste volume are the most common. These defects are shown Figure 2.

Investigations into the mechanism of these defects reveals that these are all interrelated. These defects are due to excessive solder on the board pad for the exposed die paddle of the package. During preheat and soak stage in reflow, solvents and other volatile components of the solder flux are emitted. At this stage, emitted gases, trapped between the component and the board, push the paste outwards until they are released. With the paste spread out of the pad at reflow, the solder outside the solderable surface forms solder beads. Pasting that bridge with the other leads results in an increase in volume in those leads, resulting in package tilt and imbalance in paste volume on every lead. Figure 3 shows how much the solder paste spreads during this stage of the reflow process.

The second effect of having excessive paste on the exposed die pad is that the outgassing of the flux pushes the molten solder out of the board pad and forms beads. This effect also results in voiding in the solder joint. With this, the reflow profile plays an important role. Paste manufacturers most often require preheating and soaking. These conditions allow fluxes to fully outgas so there is minimal outgassing of the flux during the reflow stage.

III. EXPERIMENTATION AND DISCUSSION
Fig. 2. Common defects observed on excessive solder on the exposed die pad–board connection. (a) Tilted, with open connection at Pin 4, (b) solder bridging, (c) x-ray photo showing solder beading under the package, (d) solder beading at the periphery of the package, (e) and (f) imbalanced solder volume on the leads’ solder joint.

Fig. 3. Product I-1 solder paste spread during reflow ramp.

To determine the appropriate stencil design for the PQFN package, several aperture designs were evaluated. These designs are listed in Tables I and II. Photos of the printed paste using these stencils are shown in Figures 4 and 5. These designs also follow the recommendation of the IPC standard for the exposed die pads. The stencil designs are arrayed into several smaller apertures with sizes varying from about 0.50mm to about 1.50mm, 0.20mm apart. Each array corresponds to a certain area reduction from the exposed die pad. The stencil thicknesses are evaluated in combination with different aperture sizes. These stencil thicknesses are 0.10mm, 0.15mm, and 0.20mm.

The materials and equipment used in this study are product I-1 solder paste, laser-cut stainless-steel stencil, FR4 boards with 36-micrometer thick copper (1 ounce/ft²) and non-solder-mask-defined pad (NSMD), vendor P-1 solder paste printer, vendor S-1 component mounter, and vendor B-1 reflow oven with air environment.

Fig. 4. (a) 6x5 array (61%), (b) 4x3 array (76%), and (c) 3x2 array (85%).

| TABLE I  
Land Footprint and Stencil Aperture Design for the Leads of PQFN 3x3 and PQFN 5x6 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Type</td>
<td>Lead Pitch (mm)</td>
<td>Land Footprint Length (mm)</td>
<td>Land Footprint Width (mm)</td>
<td>Aperture Length (mm)</td>
<td>Aperture Width (mm)</td>
</tr>
<tr>
<td>PQFN 3x3</td>
<td>0.65</td>
<td>0.70</td>
<td>0.40</td>
<td>0.65</td>
<td>0.35</td>
</tr>
<tr>
<td>PQFN 5x6</td>
<td>1.27</td>
<td>1.27</td>
<td>0.61</td>
<td>1.22</td>
<td>0.56</td>
</tr>
</tbody>
</table>

| TABLE II  
Land Footprint and Stencil Aperture Design for the Exposed Die Pad |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Type</td>
<td>Land Footprint Length (mm)</td>
<td>Land Footprint Width (mm)</td>
<td>Aperture Length (mm)</td>
<td>Aperture Width (mm)</td>
<td>Window Pane or Array (not incl. Pins 5 to 8)</td>
</tr>
<tr>
<td>PQFN 3x3</td>
<td>2.15</td>
<td>2.37</td>
<td>0.60</td>
<td>0.60</td>
<td>3x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.73</td>
<td>0.64</td>
<td>3x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.75</td>
<td>1.06</td>
<td>2x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.65</td>
<td>1.06</td>
<td>2x1</td>
</tr>
<tr>
<td>PQFN 5x6</td>
<td>4.52</td>
<td>3.91</td>
<td>0.58</td>
<td>0.48</td>
<td>6x5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.10</td>
<td>0.82</td>
<td>4x3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.76</td>
<td>1.17</td>
<td>3x2</td>
</tr>
</tbody>
</table>
Fig. 5. (a) 3x2 array (59%), (b) 3x2 array (72%), (c) 2x2 array, and (d) 2x1 array.

Fig. 6. Visual inspection results for PQFN 5x6.

Fig. 7. Visual inspection results for PQFN 3x3.

Results show that for a PQFN 3x3, the 0.60mm by 0.60mm aperture array yields a clean result. This is the aperture design with the biggest reduction relative to the exposed die pad. Similarly for the PQFN 5x6, the smallest aperture design also yields a good result. Figures 6 and 7 show the summary of the test results. None of the different apertures evaluated for both PQFN 3x3 and PQFN 5x6 showed tilted units.

Comparing the degree of solder voiding for the exposed die pad, those units that used thin stencils (0.10mm) and small apertures have the largest amount of voids. A graphical comparison of the void performance is shown in Figures 8 and 9.

B. Different Paste Evaluation

With the results of the different apertures sizes study using product I-1, a second evaluation was conducted to verify the results using pastes from other vendors. The pastes evaluated are those recommended by the manufacturer of the PQFN. These pastes are listed in Table III. One additional solder paste with leaded solder alloy was evaluated.

Reflow parameters were set to meet the temperature profiles recommended for these pastes. The three aperture designs and a stencil thickness of 0.15mm and 0.2mm were used. The
results showed better performance than the product I-1 paste. Solder beading is observed on the H-1 paste using the 4x3 array stencil aperture design, however, it is still significantly lower than the I-1 paste. No defects are observed on the K-1 and E-1 solder pastes. Similarly, no defects are seen on product I-2 and I-3 solder pastes. Void level is highest for the product I-2 and the other pastes are comparable with product I-1.

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>Different solder pastes evaluated in PQFN 5x6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product Code</td>
<td>Paste Description</td>
</tr>
<tr>
<td>Product I-1</td>
<td>SAC387 alloy, Type 3, ROL0</td>
</tr>
<tr>
<td>Product I-2</td>
<td>SAC387 alloy, Type 3, ROL0</td>
</tr>
<tr>
<td>Product I-3</td>
<td>Sn63Pb37 alloy, Type 3, ROL0</td>
</tr>
<tr>
<td>Product K-1</td>
<td>SAC387 alloy, Type 3, ROL0</td>
</tr>
<tr>
<td>Product H-1</td>
<td>SAC387 alloy, Type 3, ROL0</td>
</tr>
<tr>
<td>Product E-1</td>
<td>SAC387 alloy, Type 3, ROL0</td>
</tr>
</tbody>
</table>

C. Component Placement

The PQFN package is evaluated on its placement height. This shows the effect of compressing the paste during component placement. Two different heights were simulated; the first set of material barely compressed the printed product I-1 solder paste of 6-mils thick and the other compressed the paste to about half of its thickness. Figure 10 shows compressed solder paste after placement.

After placement, the assembly is sent to reflow and inspection. Solder beading is observed on the leg with the compressed paste. With this result, it is necessary that the placement height is controlled and not to compress the paste. Compression restricts volatiles from flowing out easily at the spaces in between print, thus pushing the paste outside the board pad. Certain component mounters have the capability to control the amount of force applied during placement, and there are other mounters that can control the height. It is best for the PQFN package and similar types of packages to be characterized to set the acceptable placement height and force.

D. Reflow Process

Both PQFN 5x6 and 3x3 were evaluated on how they respond to offset placement. The packages were intentionally placed offset relative to the board pad by 25% and 50% of the package lead width. The offset placement is 0.20mm and 0.10mm for the PQFN 5x6, and 0.16mm and 0.08mm for the PQFN 3x3. Photos of the offset units before and after reflow are shown in Figure 11.

Results show that the component actually self-aligns with the board land pad. The surface tension from the solder between the exposed thermal pad and the board pad causes the entire unit to align with the board footprint.
component board footprint. This enables checking the actual temperature to which the component is exposed. In most applications where large, thick boards are being used like motherboards with multiple layers copper, the components placed in densely populated areas of the board, in most cases, are exposed to low temperature reflow. As a result, poor soldering occurs. This poses a reliability risk in the field. For parts placed on less dense locations of the board, these are exposed to a much higher reflow temperature, which can impact the reliability of the component structure. It is imperative that during creation of reflow process conditions, areas prone for high and low peak temperatures be checked. It is also necessary to identify components that are more sensitive to reflow temperatures. Thermocouples should be placed on the component land pad to check the actual temperature of the pad. Since mounting boards respond to reflow temperature differently depending on their design, a specific set of oven parameters were created for each design in evaluating the PQFN package. This is to come up with the same temperature profile. Figure 12 shows some of the boards used to evaluate the PQFN package.

![Fig. 12. Mounting boards for PQFN, reliability test board, temperature cycle board, and thermal resistance board.](image)

Following the JEDEC standard for MSL classification, these two PQFN packages are tested and guaranteed to perform reliably to reflow conditions reaching up to 260°C peak temperatures.

**E. Board-Level Stress Tests**

Board-level stress tests were performed on the PQFN 5x6 and PQFN 3x3 packages. The tests performed are based on the qualifying standard set by Fairchild Semiconductor and on existing industry standards. The tests performed and conditions used are listed in Table IV. In compliance to referenced international standards, daisy chain PQFN 3x3 parts and boards were built. The daisy chain net included the four leads of the package. Land pads and stencil aperture used in the test are described in Table I.

**Table IV: Board-Level Tests on the PQFN**

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Reference Standard</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycle Test (using functional device)</td>
<td>FSC-QAR-0006 (Internal Qual. Standard)</td>
<td>Passed</td>
</tr>
<tr>
<td>Temperature Cycle Test (using daisy chain package)</td>
<td>IPC9701</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>No data yet</td>
</tr>
<tr>
<td>Drop Test</td>
<td>JESD22-B111</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>No data yet</td>
</tr>
<tr>
<td>Bending Cycle Test</td>
<td>JESD22-B113</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>No data yet</td>
</tr>
<tr>
<td>Vibration Test</td>
<td>JESD22-B103B</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>No data yet</td>
</tr>
</tbody>
</table>

Both PQFN 3x3 and PQFN 5x6 passed the tests. In the temperature cycle, there were no shifts greater than 25% in the electrical parameters of the device and no readings fell outside of the parametric limits. For the daisy chain PQFN 3x3, no intermittent open failures were detected by the event detector for the temperature and bend cycle tests, and the total resistance of the daisy chain network increased by less than 20% for all the units drop and vibration tested.

Cross section on units that went through the temperature cycle test showed solder cracks initiating at the toe side of the lead’s solder joint.
While cross section on the units that went through drop test, vibration and bending tests showed clean solder joints, no solder cracks were seen on the cross-sectioned units. Figure 13 shows cross-sectioned gate leads after completion of the tests.

The units were assembled using product I-1, with peak reflow temperatures between 240°C to 250°C in an air environment. Small solder fillets on the side wall of the copper can be seen on the units reflowed in an air environment. This structure is acceptable and passes reliability tests. IPC-A-610 standard requires such structure as a minimum for no-lead type packages.

F. Thermal Resistance Measurement and Board Design

With large voids observed on the exposed die pad of the package, it is necessary to understand its impact on thermal performance of the package.

Two board designs were used to determine the impact of solder voids in the exposed die pad to the thermal resistance of the package. The first board has a 1 square inch copper ground plane 71 micrometers thick (2 ounce/ft²) to dissipate heat; the other board design has a minimum pad size. Figure 14 shows board designs used in the study.

Different levels of voiding are built by altering the printed paste volume and reflow parameters. Void levels from 10% to 80% were assembled. Using a semiconductor thermal analyzer from ANALYSIS TECH™, representative voids using the two board designs were used for junction calibration of the device to determine the relationship between temperature and the voltage across the junction of the device. The average value of the slope relating the two parameters was used in determining the thermal resistance of the package for these two board types. Figure 15 shows the equipment used for the junction calibration. The device is immersed in inert thermal oil and is constantly stirred to achieve uniformity in temperature of the bath.

Fig. 13. Cross-sections of PQFN 3x3 package through the gate lead, where the package occupies the upper right portion of the photograph, after: (a) temperature cycle test (-40/125°C test condition), (b) drop test, and (c) bending cycle test.

Fig. 14. (a) Minimum board pad and (b) 1 square inch board pad.

Fig. 15. Device junction calibration (left) and thermal resistance chamber (right).
The units are then tested in a thermal resistance chamber, shown in Figure 15. By applying continuous heating power to the device, the device junction temperature is measured. Thermal resistance is defined by the following equation once steady-state thermal equilibrium is reached:

$$\theta_{JA} = \left( T_J - T_A \right) / P$$

where \( T_J \) is the junction temperature (°C), \( T_A \) is the ambient temperature (°C), \( P \) is the heat dissipation (watts), and \( \theta_{JA} \) is thermal resistance junction-to-ambient temperature (°C/watt).

Lower \( \theta_{JA} \) indicates better thermal performance. Figure 15 shows the thermal resistance measurement setup with a thermal camera to verify the temperature gradients along the package surface.

The results from the experiment showed that the thermal resistance from device junction to the ambient temperature (\( \theta_{JA} \)) on units with different level of voids (10%-80%) showed no significant effect on the thermal performance of the package using the two board designs. Figures 16 and 17 shows a plot of the measured thermal resistance.

A commercial finite element analysis tool, ANSYS®, is used to verify the experimental results. Using computer simulation, parameters such as void location, distribution, void size, and bond-line thickness can be analyzed one factor at a time. Steady-state thermal analysis is conducted using a 1 inch square pad and a minimum pad PWB to look at the effect on the thermal resistance due to the presence of voids after board mounting.

The package and PWB are drawn in 3D using CAD software to represent the actual geometry. Standard thermal conductivities of the various materials of the package and the PWB are input into the model. The materials are assumed in the model to have isotropic thermal behavior and are perfectly attached together except in areas where voids are intentionally placed. For heat generation, the power is applied to the volume of the silicon die. Temperature dependent convection boundaries are placed on the top, sides, and bottom surfaces for the software to calculate the appropriate heat transfer across the specified surfaces.
Fig. 19. Temperature distribution of the assembly with the FR4 material hidden. Maximum temperature occurs at the package top, directly above the die, and the minimum temperature is located at the socket region.

The model is initially calibrated to match the experimental result. The socket affects the temperature distribution of the package as it draws out heat by conduction. To include the effect of the socket, surface loads are applied and adjusted to correlate with actual readings. After the boundary conditions have been set, a void model is arbitrarily created using five (5) circular voids to represent variations in void size and distribution for different void percentages. As the void percentage is increased for the study, circular voids cannot be created without overlapping each other, so four (4) rectangular voids replaced the five (5) circular voids. The result of the modeling showed the same outcome with the experimental study - there is no significant effect in steady-state thermal performance even up to 80% of voids occurring at the board solder. The modeling study extended the percentage of voids until 98% and θ_JA dramatically increased only after 80%. Figure 20 shows the graph of the thermal resistance versus the void percentage.

Next, the void size and distribution is changed and investigated. Instead of the five circular voids, 20 smaller circular voids are created maintaining the same total percentage. Figure 21 shows the comparison of the void size and distribution. The result remains the same; there was no significant change in the thermal resistance.

Fig. 21. Illustration of the two different tests in void size and distribution. Figure on the left side has five large circular voids, while the right figure has 20 smaller circular voids. Both totaled 30% voids.

The study was continued by examining the effect of thermal resistance when the solder joint thickness is changed. The previous modeling studies have a joint thickness of 2.56mils, an average value taken from measuring the actual builds. For a joint thickness difference of 1.28mils (or 32µm), the result showed minimal difference in thermal resistance of approximately 0.37°C/W.

G. Effect of Thermal Vias in Pad in the Thermal Resistance Performance of the PQFN Package

In some board designs, ground planes on the board are provided to serve as a thermal path during operation to dissipate heat. The ground plane is at times located in different layers of the board and, in most cases, this is either at the top or bottom side of the board.

An experiment was conducted to check improvement in the thermal resistance of the PQFN 5x6 package by adding thermal vias in the board pad for the exposed die pad of the package and connected to the backside of 1.60mm thick board with 1 square inch copper trace at the backside of the board, 71 micrometers thick copper (2 ounce/ft²). The number of vias is varied from 2 to 12 in order to compare improvement in the thermal resistance. The via-hole size has a diameter of 0.30mm and 0.036mm copper plating. It should be noted, however, that the 1 square inch
copper trace is selected to establish a comparison to the 1 square inch board used in the evaluation on void effects, and that this should not be used as guideline for customer’s board design, but as a reference only.

Fig. 22. Via-in-pad board for PQFN 5x6 with four vias in pad showing enlarged view of the pad and the board backside.

Fig. 23. Via-in-pad boards for PQFN 5x6; (a) two vias, (b) six vias, (c) nine vias, and (d) 12 vias.

Results of the test showed that adding vias-in-pad improves the thermal resistance of the assembly. The thermal resistance value decreases with an increasing number of thermal vias-in-pad. Significant improvement is observed from two to four vias-in-pad. Results are shown in Figure 24. In the graph, note that the improvement decreases as the number of vias increases.

Alternative options that can be used in lieu of through-hole vias, include the use of vias filled with conductive epoxy and copper plated to completely fill a solderable pad surface. Tenting and plugging are other options.

Fig. 24. Thermal resistance with different number of vias in pad.

Fig. 25. Via-in-pad with printed paste on pad. There is a 0.30mm overlap on the aperture design, not directly printing on the via.

Fig. 26. X-ray showing voids and vias filled with solder; (a) four vias in pad and (b) nine vias in pad.

- It has been demonstrated that solder voids of up to 80% between the board pad and the exposed die paddle does not impact the thermal performance of the package. The use of through-hole vias only increases the amount of voids. However, with the learnings from the above evaluations, voiding should not be a concern. Depending on the board design particularly on the number of layers and thickness of the board used, reliability of the vias should be tested. This is to guarantee there will be no related failures experienced in the field.
IV. CONCLUSION

This paper presents board-level evaluations of PQFN packages. The main points of the study are:

Stencil Aperture Design:

• Reduction in stencil aperture size for the exposed die pad of PQFN package is necessary; the resulting print coverage is between 50 to 80% of the board pad. For product I-1, the print coverage is about 60%.
• Reduction in stencil aperture may depend on the solder paste being used and its behavior during reflow. It is best that the paste be evaluated to understand its behavior during reflow.
• The reduced aperture for PQFN packages works well with different stencil thicknesses. This has been demonstrated with the clean inspection results for the three stencil thicknesses evaluated. However, the board assembler should be cautious in using thick stencil since the increase in volume of printed paste proportionally increases the volume of flux, which results in increased gas emission at reflow. In such cases, reflow profile should be carefully characterized.
• Window paning the aperture for the exposed die pad is recommended; this allows volatile components of the solder flux to be released, minimizing void formation. This also prevents the solder paste from spreading.

Component Placement:

• Controlling the placement height is necessary. This should be maintained such that the height does not squash the printed solder paste. Squashed printed paste prevents outgassing of the flux’s volatile components and leads to defects. The height can be set by controlling the amount of force or the placement height during component mounting. Equipment available in the market has the capability for controlling placement.
• X and Y placement should be limited to 0.20mm for the PQFN 5x6 and 0.16mm for the PQFN 3x3. The component self-aligns with this amount of placement offset. This limit is not as critical since most component mounters have a placement accuracy better than 0.10 mm.

Reflow Conditions

• It is critical to control the temperature to which the PQFN packages are exposed. Exposing the package to temperatures above 260°C can risk the reliability of the component, while exposure to low temperatures can inhibit formation of good solder joints. It is recommended that when temperature reflow parameters are being set, thermocouples be placed on the component pad. This will measure the actual temperature to which the component is being subjected. It has been demonstrated that different boards respond differently to the same reflow parameters. As a result, a different set of parameters may have to be set for each board.

Board-Level Stress Test

• PQFN has passed the standards set by Fairchild and the industry. The results show that these two PQFN packages can meet the expected performance in the field. This is with the use of lead-free solder alloy (SAC387) and with solder interconnection at the bottom side of the lead only. This is in agreement with the accepted solder joint structure for a PQFN package described in IPC-A-610. Wetting on the side wall of the sawn terminations is not necessary.

Effects of Solder Voids on the Exposed Die Pad of the Package to Thermal Resistance

• Voids do not significantly impact the thermal resistance of the package mounted in a minimum copper pad or on a 1 square inch pad.
• Although an increasing trend in the thermal resistance is seen in FEA for void levels greater than 80%, this should not be a concern, since it is unlikely to get this many voids in assembly.
• Solder joint reliability should not be a concern on the exposed die pad of the component; it has been demonstrated in board-level stress tests that even on a relatively small solder joint on the leads, these did not result in failure.
• More tests are still recommended, however, to check the impact of voids to the transient response or thermal impedance of the package.
**Thermal Vias-in-Pad**

- Thermal vias-in-pad are recommended for designs with ground layers on other layers of the board, serving as a thermal path for heat dissipation.
- Using through-hole vias, voiding should not be a concern; it has been demonstrated that voids below 80% do not impact the thermal performance of the package. Due to the solder wicking through the vias, however, board designers should be cautious that no components be placed directly on the opposite side of the board, which can potentially result in bridging and electrical shorting of the assembly. A solder mask should be used on the opposite side of the board. A copper pad concentric to the hole should be formed so as not to allow solder spreading at the opposite side of the board and to provide tolerance between the hole and solder mask opening. Other alternatives to through-hole vias are available, such as filling the via with conductive adhesive and plating the structure with copper, creating a solderable pad on the via.
- More studies are recommended; such studies should focus on optimizing the size, number, and locations of the via-in-pad and determining resulting reliability.

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